WHAT IS CLAIMED IS:

1. A reset control system for a system having a central processing section and a peripheral control section which are formed on separate chips, said reset control system comprising:

a system reset output section for generating and outputting a system reset signal on the basis of an external reset signal and an emulator reset signal based on a reset instruction from an emulator for independently implementing a function of said central processing section,

wherein said system reset signal output from said system reset output section is supplied to both chips of said central processing section and said peripheral control section.

2. A reset control system according to claim 1, wherein said system reset signal is generated by OR-operating said emulator reset signal and said external reset signal.

3. A reset control system according to claim 1, wherein said system reset output section is provided in the chip of said peripheral control section.

4. A reset control system according to claim 1, wherein said system reset output section is provided in the chip of said central processing section.

5. A reset control system according to claim 1, further comprising a mask processing section for masking said external reset signal when said emulator

is in operation.

6. A reset control system according to claim 1, further comprising a synchronization processing section for synchronizing activation timings after reset between said central processing section and said peripheral control section, said synchronization processing section being formed on at least one of the chips of said central processing section and said peripheral control section.

7. A reset control system according to claim 6, wherein said synchronization processing section comprises an activation enable signal output section for outputting an activation enable signal for instructing to enable activation after elapse of a predetermined time after reset of said central processing section or said peripheral control section.

8. A reset control system according to claim 5, further comprising a synchronization processing section for synchronizing activation timings after reset between said central processing section and said peripheral control section, said synchronization processing section being formed on at least one of the chips of said central processing section and said peripheral control section.

9. A reset control system according to claim 8, wherein said synchronization processing section comprises an activation enable signal output section for outputting an activation enable signal for

instructing to enable activation after elapse of a predetermined time after reset of said central processing section or said peripheral control section.

10. A reset control system for a system having a central processing section and a peripheral control section which are formed on separate chips, said reset control system comprising:

a reset selection section for selectively outputting, as a system reset signal, one of an external reset signal and an emulator reset signal based on a reset instruction from an emulator for independently implementing a function of said central processing section,

wherein said system reset signal output from said reset selection section is supplied to both chips of said central processing section and said peripheral control section.

11. A reset control system according to claim 10, further comprising a synchronization processing section for synchronizing activation timings after reset between said central processing section and said peripheral control section, said synchronization processing section being formed on at least one of the chips of said central processing section and said peripheral control section.

12. A reset control system according to claim 11, wherein said synchronization processing section comprises an activation enable signal output section

for outputting an activation enable signal for instructing to enable activation after elapse of a predetermined time after reset of said central processing section or said peripheral control section.

13. A reset control system for a system having a central processing section, said reset control system comprising a mask processing section for masking an external reset signal when an emulator for independently implementing a function of said central processing section is in operation.

14. A reset control method for a system having a central processing section and a peripheral control section which are formed on separate chips, said method comprising the steps of:

masking an external reset signal when an emulator for independently implementing a function of said central processing section is in operation;

generating a system reset signal on the basis of the masked external reset signal and an emulator reset signal based on a reset instruction from said emulator; and;

supplying said system reset signal to both chips of said central processing section and said peripheral control section.

15. A method according to claim 14, wherein said system reset signal is generated by OR-operating said emulator reset signal and said masked external reset signal.

16. A reset control method for a system having a central processing section and a peripheral control section which are formed on separate chips, said method comprising the steps of:

selectively outputting, as a system reset signal, one of an external reset signal and an emulator reset signal based on a reset instruction from an emulator for independently implementing a function of said central processing section; and

supplying said system reset signal to both chips of said central processing section and said peripheral control section.